University of Bahrain
CE -- CIT -- UOB
TEST 2 (13 May 2015) ITCE 444: µP-Based Design

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Time: 60 minutes

Note: Throughout the following two questions, the µC clock frequency is kept @ 8 MHz.

Q1. [60 marks]

The following program generates a square wave at bit 7 of port D:

a) Find the frequency of the generated wave
b) Make changes in the program to get minimum frequency. Find this frequency.
c) Make changes in the program to get maximum frequency. Find this frequency.
d) What hardware and software changes will make the frequency = 1 cycle/hour ?

```
        BCF    TRIS ,
        MOVLW  0x
        MOVWF  T0CON
HERE    MOVLW  0x
        MOVWF  TMR0H
        MOVLW  0x
        MOVWF  TMR0L
        BCF    INTCON, TMR0IF
        BTG    PORT ,
        BSF    T0CON, TMR0ON
AGAIN   BTFSS  INTCON, TMR0IF
        BRA    AGAIN
        BCF    T0CON, TMR0ON
        BRA    HERE
```

Q2. [40 marks]

Assume 3 ideal **2 mV/°C** linear temperature sensors are connected to 3 channels of the µC 10-bit ADC where V_{REF} = 0.6 volt:

a) Which **pins** would you use for the 3 channels and V_{REF} ?
b) When you are processing the **second** temperature sensor, what values for the registers ADCON0 and ADCON1 will you write?
c) Find the temperature range covered.
d) Find the temperature resolution.
e) Find the temperature if the ADC reading is 07F.
f) What will be ADC reading at 35 °C?

TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0

TMR0ON D7 Timer0 ON and OFF control bit
1 = Enable (start) Timer0
0 = Stop Timer0

T08BIT D6 Timer0 8-bit/16-bit selector bit
1 = Timer0 is configured as an 8-bit timer/counter.
0 = Timer0 is configured as a 16-bit timer/counter.

T0CS D5 Timer0 clock source select bit
1 = External clock from RA4/T0CKI pin
0 = Internal clock (Fosc/4 from XTAL oscillator)

T0SE D4 Timer0 source edge select bit
1 = Increment on H-to-L transition on T0CKI pin
0 = Increment on L-to-H transition on T0CKI pin

PSA D3 Timer0 prescaler assignment bit
1 = Timer0 clock input bypasses prescaler.
0 = Timer0 clock input comes from prescaler output.

T0PS2:T0PS0 D2D1D0 Timer0 prescaler selector

0 0 0 = 1:2	Prescale value (Fosc / 4 / 2)
0 0 1 = 1:4	Prescale value (Fosc / 4 / 4)
0 1 0 = 1:8	Prescale value (Fosc / 4 / 8)
0 1 1 = 1:16	Prescale value (Fosc / 4 / 16)
1 0 0 = 1:32	Prescale value (Fosc / 4 / 32)
1 0 1 = 1:64	Prescale value (Fosc / 4 / 64)
1 1 0 = 1:128	Prescale value (Fosc / 4 / 128)
1 1 1 = 1:256	Prescale value (Fosc / 4 / 256)

ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	--	ADON

ADCS2 (from ADCON1)	ADCS1	ADCS0	Conversion Clock Source
0	0	0	Fosc/2
0	0	1	Fosc/8
0	1	0	Fosc/32
0	1	1	Internal RC used for clock source
1	0	0	Fosc/4
1	0	1	Fosc/16
1	1	0	Fosc/64
1	1	1	Internal RC used for clock source

CHS2	CHS1	CHS0	CHANNEL SELECTION	
0	0	0	CHAN0 (AN0)	
0	0	1	CHAN1 (AN1)	
0	1	0	CHAN2 (AN2)	
0	1	1	CHAN3 (AN3)	
1	0	0	CHAN4 (AN4)	
1	0	1	CHAN5 (AN5)	not implemented on 28-pin PIC18
1	1	0	CHAN6 (AN6)	not implemented on 28-pin PIC18
1	1	1	CHAN7 (AN7)	not implemented on 28-pin PIC18

GO/DONE A/D conversion status bit.
1 = A/D conversion is in progress. This is used as start conversion, which means after the conversion is complete, it will go LOW to indicate the end-of-conversion.
0 = A/D conversion is complete and digital data is available in registers ADRESH and ADRESL.

ADON A/D on bit
0 = A/D part of the PIC18 is off and consumes no power. This is the default and we should leave it off for applications in which ADC is not used.
1 = A/D feature is powered up.

ADFM	ADCS2	--	--	PCFG3	PCFG2	PCFG1	PCFG0

ADFM A/D Result format select bit

1 = Right justified: The 10-bit result is in the ADRESL register and the lower 2 bits of ADRESH. That means the 6 most significant bits of the ADRESH register are all 0s.

0 = Left justified: The 10-bit result is in the ADRESL register and the upper 2 bits of ADRESL. That means the 6 least significant bits of the ADRESL register are all 0s.

ADCS2 A/D Clock Select bit 2. This bit along with the ADCS1 and ADCS0 bits of the ADCON0 register decide the conversion clock for the ADC. The default value for ADCS2 is 0, which means setting the ADCS0 and ADCS1 values of ADCON0 can give us clock conversion of Fosc/2, Fosc/8, and Fosc/32. See the ADCON0 register.

PCFGs: A/D Port Configuration Control bits:

PCFGs	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	Vref+	Vref-	C/R
0 0 0 0	A	A	A	A	A	A	A	A	Vdd	Vss	8/0
0 0 0 1	A	A	A	A	Vref+	A	A	A	AN3	Vss	7/1
0 0 1 0	D	D	D	A	A	A	A	A	Vdd	Vss	5/0
0 0 1 1	D	D	D	A	Vref+	A	A	A	AN3	Vss	4/1
0 1 0 0	D	D	D	D	A	D	A	A	Vdd	Vss	3/0
0 1 0 1	D	D	D	D	Vref+	D	A	A	AN3	Vss	2/1
0 1 1 x	D	D	D	D	D	D	D	D	-	-	0/0
1 0 0 0	A	A	A	A	Vref+	Vref–	A	A	AN3	AN2	6/2
1 0 0 1	D	D	A	A	A	A	A	A	Vdd	Vss	6/0
1 0 1 0	D	D	A	A	Vref+	A	A	A	AN3	Vss	5/1
1 0 1 1	D	D	A	A	Vref+	Vref–	A	A	AN3	AN2	4/2
1 1 0 0	D	D	D	A	Vref+	Vref–	A	A	AN3	AN2	3/2
1 1 0 1	D	D	D	D	Vref+	Vref–	A	A	AN3	AN2	2/2
1 1 1 0	D	D	D	D	D	D	D	A	Vdd	Vss	1/0
1 1 1 1	D	D	D	D	Vref+	Vref–	D	A	AN3	AN2	1 /2

A = Analog input, D = Digital I/O

C/R = # of analog input channels / # of pins used for A/D voltage reference

The default is option 0000, which gives us 8 channels of analog input and uses the Vdd of PIC18 as Vref.